

Galatea IO Expansion Module User Guide

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Introduction

This board is an IO breakout solution for Galatea Spartan 6 PCI Express FPGA Board. This product allows Galatea's IOs to be broken out in to smaller 2x6 headers that would facilitate easy attachment of other peripheral expansion modules. The board features seven 2x6 expansion connector. Please note that the external power connector on Galatea PCI Express FPGA Development Board will not be accessible when this module is placed the high speed IO connector P5.

Board features

- Seven 2x6 pin expansion connectors
- Can be attached to either side of Galatea FPGA board
- Dimension: 56.64mm X 110.99mm

How to use the module

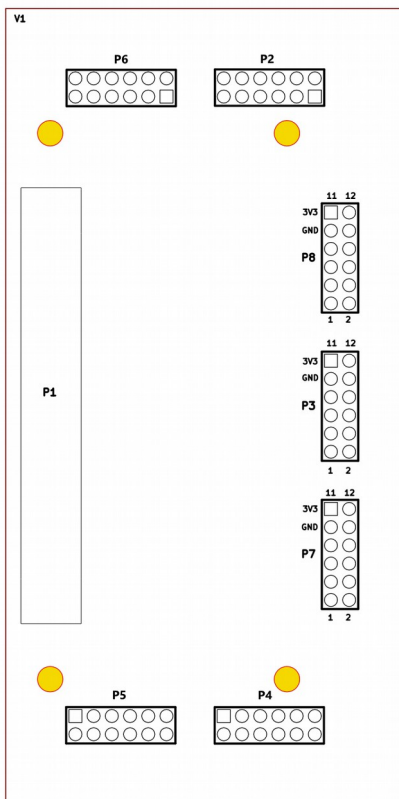
The following section describes how to use this module.

Components/Tools required

Along with the module, you may need the items in the list below for easy and fast installation.

1. Galatea FPGA Development Board.

Connection Diagram



This diagram should be used as a reference only. For detailed information, see the schematics at the end of this document. Details of individual connectors are as below.

Connection Details

IO Header P2

IO Header Pin No.	Pin Detail	Header P1 Pin No.
1	IO1	92
2	IO2	93
3	IO3	95
4	IO4	96
5	IO5	98
6	IO6	99
7	IO7	101
8	IO8	102
9	GND	-
10	GND	-
11	VCC3V3	-
12	VCC3V3	-

IO Header P3

IO Header Pin No.	Pin Detail	Header P1 Pin No.
1	IO1	80
2	IO2	81
3	IO3	83
4	IO4	84
5	IO5	86
6	IO6	87
7	IO7	28
8	IO8	29
9	GND	-
10	GND	-
11	VCC3V3	-
12	VCC3V3	-

IO Header P4

IO Header Pin No.	Pin Detail	Header P1 Pin No.
1	IO1	74
2	IO2	75
3	IO3	77
4	IO4	78
5	IO5	58
6	IO6	59
7	IO7	55
8	IO8	56
9	GND	-
10	GND	-
11	VCC3V3	-
12	VCC3V3	-

IO Header P5*

IO Header Pin No.	Pin Detail	Header P1 Pin No.
1	IO1	62
2	IO2	63
3	IO3	65
4	IO4	66
5	IO5	68
6	IO6	69
7	IO7	71
8	IO8	72
9	GND	-
10	GND	-
11	VCC3V3	-
12	VCC3V3	-

IO Header P6*

IO Header Pin No.	Pin Detail	Header P1 Pin No.
1	IO1	25
2	IO2	26
3	IO3	22
4	IO4	23
5	IO5	19
6	IO6	20
7	IO7	16
8	IO8	17
9	GND	-
10	GND	-
11	VCC3V3	-
12	VCC3V3	-

IO Header P7

IO Header Pin No.	Pin Detail	Header P1 Pin No.
1	IO1	52
2	IO2	53
3	IO3	49
4	IO4	50
5	IO5	46
6	IO6	47
7	IO7	43
8	IO8	44
9	GND	-
10	GND	-
11	VCC3V3	-
12	VCC3V3	-

IO Header P8

IO Header Pin No.	Pin Detail	Header P1 Pin No.
1	IO1	89
2	IO2	90
3	IO3	37
4	IO4	38
5	IO5	34
6	IO6	35
7	IO7	31
8	IO8	32
9	GND	-
10	GND	-
11	VCC3V3	-
12	VCC3V3	-

For more information, refer the schematics at the end of this document.

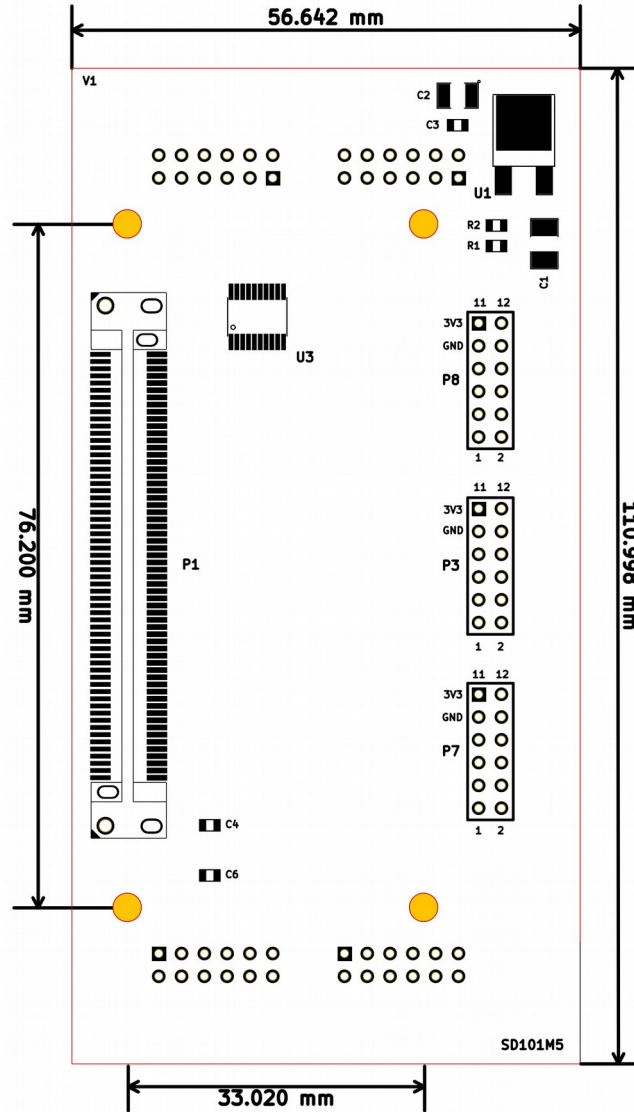
*Header P5 and P6 are connected to FPGA via a bidirectional voltage level translator, for more information kindly see the schematics.

Technical Specifications

Parameter *	Value	Unit
Basic Specifications		
Power supply voltage	3.3	V
TXB0108 (Voltage Level Translator)		
Supply Voltage (VCCA)	1.5	V
Supply Voltage (VCCB)	3.3	V
Data Rate	100	Mbps

* All parameters considered nominal. Numato Systems Pvt Ltd reserve the right to modify products without notice.

Physical Dimensions

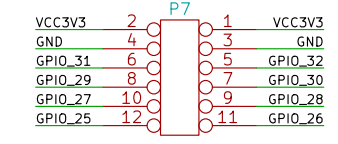
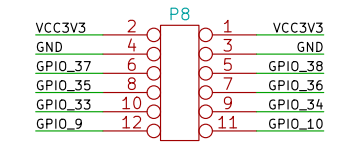
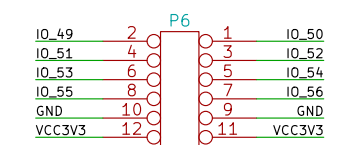
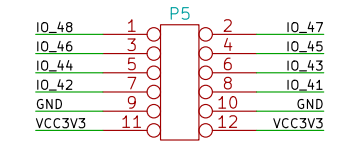
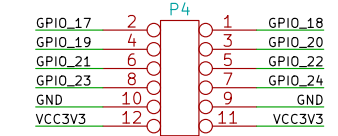
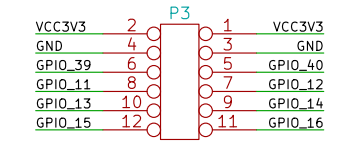
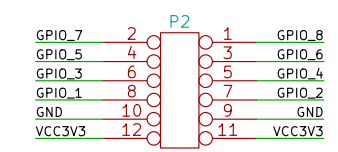
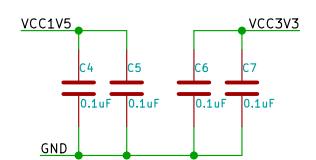
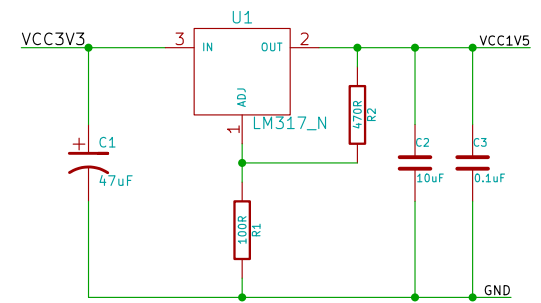
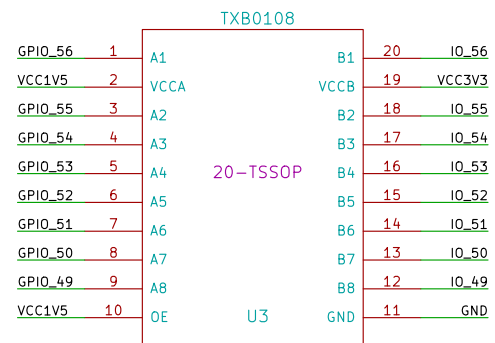
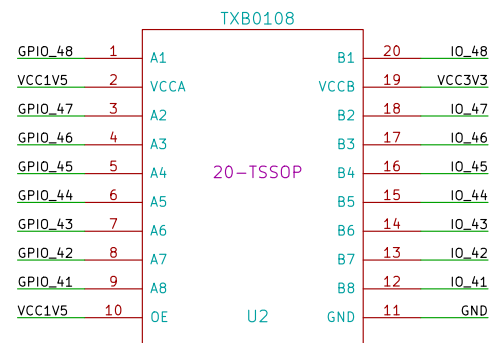
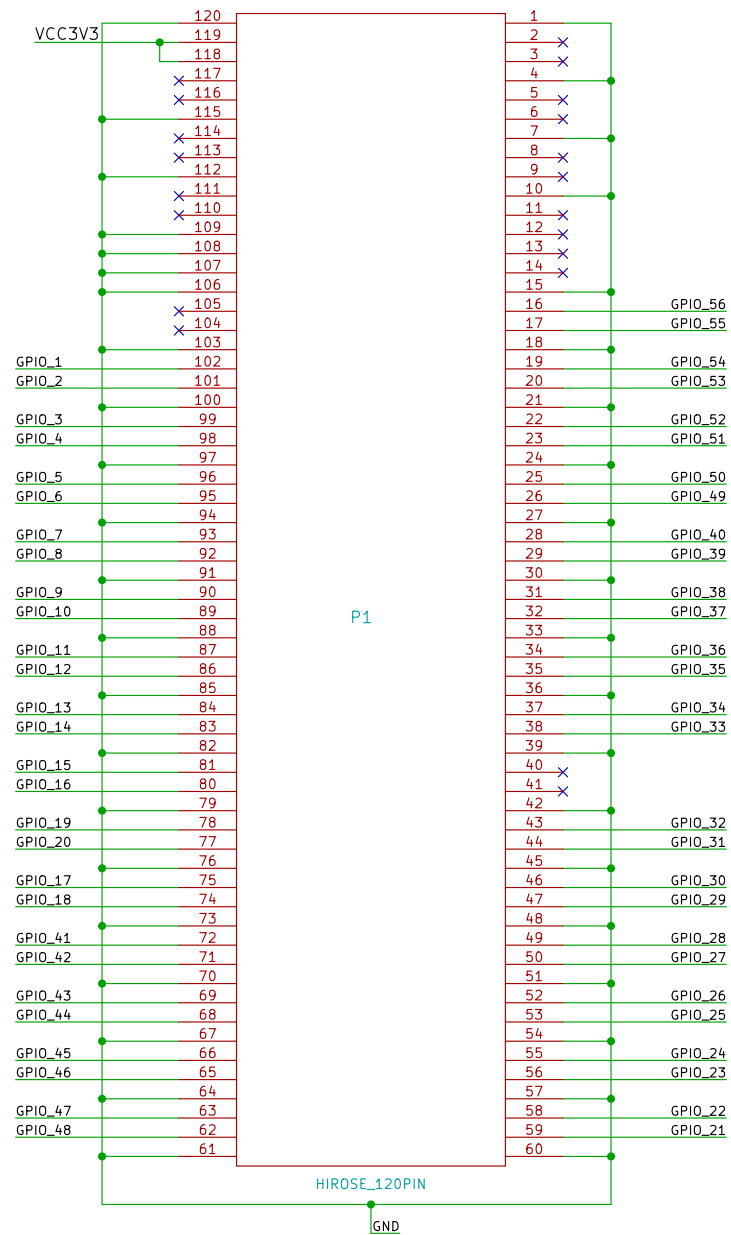


L x W x H : 110.998 mm x 56.642 mm x 11 mm

Mechanical Hole Diameter- 3.25 mm

Schematics

See next page.



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