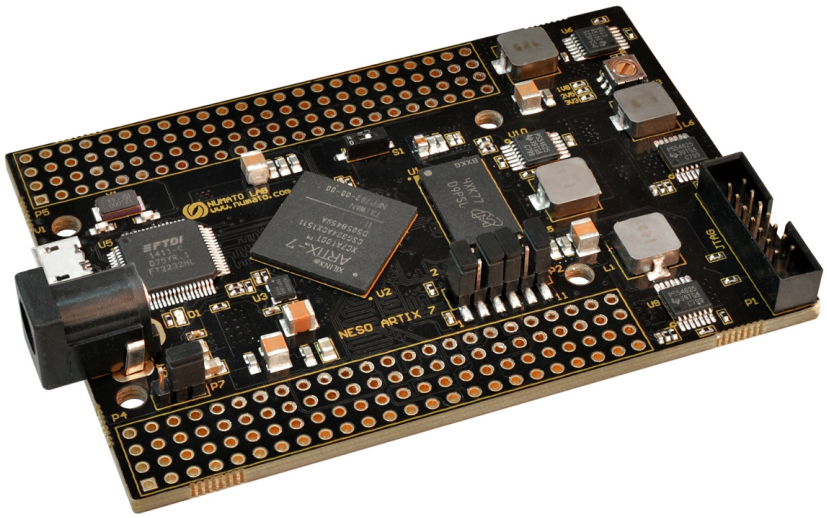

NESO Artix 7 FPGA Development Board

User Guide

NUMATO LAB

www.numato.com

Rev 1

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India

* Mail orders, phone orders and direct pick up are not available at this time. Please visit our online store to place your order. Estimated shipping time to your address will be displayed in the shopping cart before checkout.

Introduction

Neso is an easy to use FPGA Development board featuring Artix 7 FPGA. It is specially designed for development and integration of FPGA based accelerated features to other designs. This development board features Xilinx XC7A100T FPGA with FTDI's FT2232H Dual-Channel USB device. The high speed USB 2.0 interface provides fast and easy configuration download to the on-board SPI flash. No programmer or special down loader cable is needed to download the bit stream to the board.

Applications

- Product Prototype Development
- Accelerated computing integration
- Development and testing of custom embedded processors
- Signal Processing
- Communication devices development
- Educational tool for Schools and Universities

Board features

- FPGA: XC7A100T in CSG324 package
- DDR3: 2Gb DDR3 (MT41J128M16JT-125:K)
- Flash memory: 128 Mb SPI flash memory (N25Q128A13ESE40E)
- 100MHz CMOS oscillator
- High Speed USB 2.0 interface for On-board flash programming. FT2232H Channel A is dedicated for SPI Flash /JTAG Programming. Channel B can be used for custom applications.
- On-board voltage regulators for single power rail operation
- FPGA configuration via JTAG and USB
- Maximum IOs for user defined purposes
  FPGA - 140 IOs
  FT2232H - 8 IOs

How to use the module

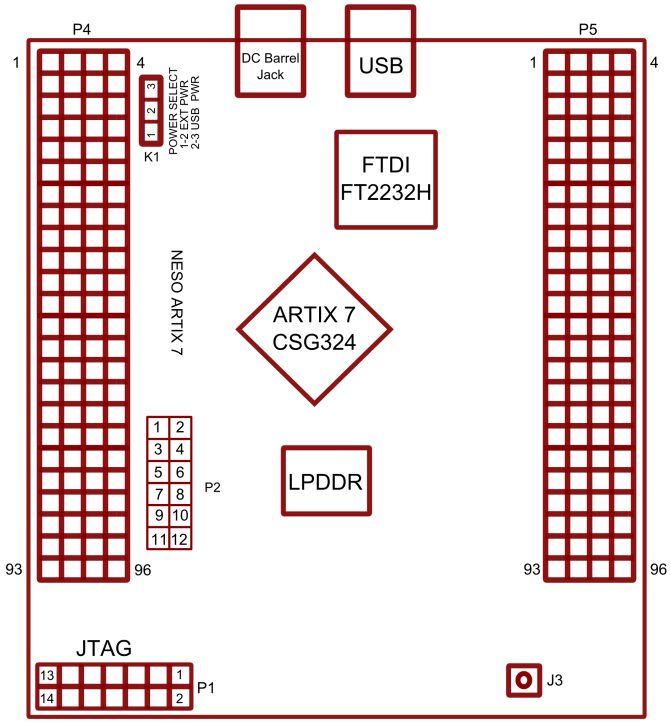
The following section describes how to use this module.

Components/Tools required

Along with the module, you may need the items in the list below for easy and fast installation.

1. USB A to Micro B cable.
2. DC Power supply (Optional).

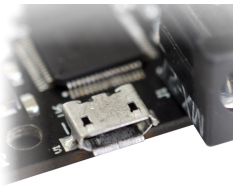
Connection Diagram



This diagram should be used as a reference only. For detailed information, see Neso schematics at the end of this document. Details of individual connectors are as below.

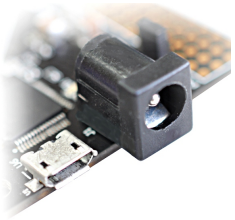
USB Interface

The on board full speed USB controller helps a PC/Linux/Mac computer to communicate with this module. Use a USB A to Micro B cable to connect with a PC. By default the module is powered from USB so make sure not to overcrowd unpowered USB hubs (the picture on the right shows USB Micro connector).



Visit http://numato.com/cables-accessories to buy cables and accessories for this product.

DC Power Supply



This module uses +5V power supply to function properly. **By default the board is configured to use +5V supply from USB. So an external +5V power is not required unless USB port is unable to supply enough current. In most cases USB ports are capable of providing enough current for the module. Current requirement for this board largely depends on your application. Please consult FPGA data sheet for more details on power requirements.** If for any reason, an external 5V power supply needs to be used for the module, the Power select jumper should be configured properly before connecting the power supply. Please refer to the marking on the board for more details.

Power Select

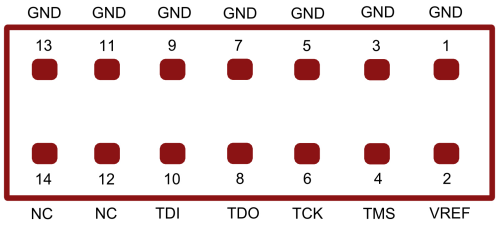
The Power Select header K1 is used to configure the power source for the board. Connect pins 2 and 3 to use USB power and pin connect pins 1 and 2 to use the external DC power.

VADJ Supply

This board is equipped with a rotary switch **(J3)** for selecting **bank 35** IO voltage level. It is possible to select 3 different voltage level for the bank ie, **1.8V, 2.5V** and **3.3V** as per the user requirement.

JTAG Connector

JTAG connector provides access to FPGA's JTAG pins. A XILINX platform cable can be used to for JTAG programming.



JTAG/SPI Configuration on FT2232H channel A

Channel A of FT2232H can be connected to the SPI bus that connects the SPI Flash chip to the FPGA or to the JTAG pins of the FPGA. By connecting SPI bus to FT2232H channel A, the SPI flash can be directly programmed to save the configuration permanently. This is the default configuration set when Neso is shipped. When FT2232H channel A is connected to SPI, Neso Configuration Downloader utility can be used to program the board.

When FT2232H channel A is connected to FPGA JTAG, the JTAG signals can be accessed directly through FT2232H. Neso Configuration Downloader utility currently does not support programming FPGA SRAM through JTAG.

Please see the tables below for information about selecting SPI or JTAG for FT2232H channel A. SPI must be selected for Neso Configuration Downloader utility to work.

Header P10

Jumper Configuration for SPI	Jumper Configuration for JTAG
1 - 2	2 - 4
5 - 6	3 - 5
7 - 8	8 - 10
11 - 12	9 - 11

GPIOs

This device is equipped with a maximum 140 user IO pins that can be used for various custom applications. All user IOs are length matched and can be used as differential pairs.

Header P4

Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin No. On The Header	Artix-7 (CSG324) Pin No.
1	GND	2	3V3
3	VCCIN	4	GND
5	A14	6	A13
7	D13	8	D12
9	A11	10	B11
11	F14	12	F13

13	B14	14	B13
15	A16	16	A15
17	A9	18	A10
19	B12	20	C12
21	A8	22	B8
23	C10	24	C11
25	B9	26	C9
27	B6	28	B7
29	C5	30	C6
31	A5	32	A6
33	C7	34	D8
35	D7	36	E7
37	D4	38	D5
39	-	40	-
41	-	42	-
43	D3	44	E3
45	-	46	-
47	A3	48	A4
49	GND	50	GND
51	GND	52	GND
53	-	54	-
55	B2	56	B3
57	C1	58	C2
59	A1	60	B1
61	G1	62	H1
63	E1	64	F1
65	-	66	-
67	D2	68	E2
69	K1	70	K2
71	J2	72	J3

73	B4	74	C4
75	E5	76	E6
77	G2	78	H2
79	F3	80	F5
81	G3	82	G4
83	H5	84	H6
85	H4	86	J4
87	F6	88	G6
89	GND	90	GND
91	GND	92	GND
93	3V3	94	3V3
95	3V3	96	3V3

Header P5

Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin No. On The Header	Artix-7 (CSG324) Pin No.
1	ACBUS0*	2	ACBUS1
3	3V3	4	GND
5	ACBUS2	6	ACBUS3
7	B16	8	B17
9	ACBUS4	10	ACBUS5
11	D14	12	C14
13	ACBUS6	14	ACBUS7
15	C16	16	C17
17	H14	18	G14
19	D15	20	C15
21	E15	22	E16
23	E17	24	D17
25	F15	26	F16
27	J14	28	H15

29	H17	30	G17
31	H16	32	G16
33	K13	34	J13
35	L15	36	L16
37	L18	38	M18
39	R12	40	R13
41	K15	42	J15
43	M16	44	M17
45	GND	46	GND
47	GND	48	GND
49	GND	50	GND
51	GND	52	GND
53	R18	54	T18
55	P15	56	R15
57	N15	58	N16
59	N14	60	P14
61	P17	62	R17
63	N17	64	P18
65	U16	66	V17
67	U17	68	U18
69	U14	70	V14
71	V15	72	V16
73	T14	74	T15
75	R16	76	T16
77	T9	78	T10
79	T13	80	U13
81	T11	82	U11
83	R10	84	R11
85	V10	86	V11
87	U12	88	V12

89	INITB	90	3V3
91	PROGB	92	3V3
93	GND	94	GND
95	GND	96	GND

* ACBUS0 - ACBUS7 are pins of FTDI FT2232H Dual-Channel USB device.

	VCC
	Ground
	GPIO
	FTDI IO

FT2232H – Artix-7 (CSG324) FPGA Connection Details

FTDI Pin No.	Pin Function (245 FIFO)	Artix-7 Pin No.
38	D0	A18
39	D1	B18
40	D2	D18
41	D3	E18
43	D4	F18
44	D5	G18
45	D6	J17
46	D7	J18
48	RXF#	G13
52	TXE#	K16
53	RD#	D9
54	WR#	M13
55	SIWUB	D10

Driver Installation

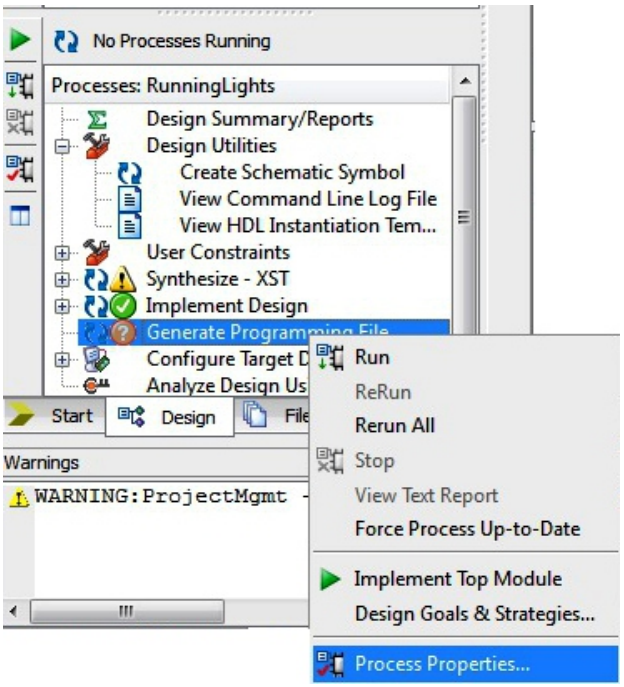
Windows

This product requires a driver to be installed for proper functioning when used with Windows. The D2XX driver can be downloaded from http://www.ftdichip.com/Drivers/D2XX.htm. Windows Users run the CDM v2.08.30 WHQL Certified.exe application that will prompt to install the FTDI CDM drivers. When driver installation is complete, the module should appear in Neso Flash Config Tool as Neso Artix-7 FPGA Module (see the picture).

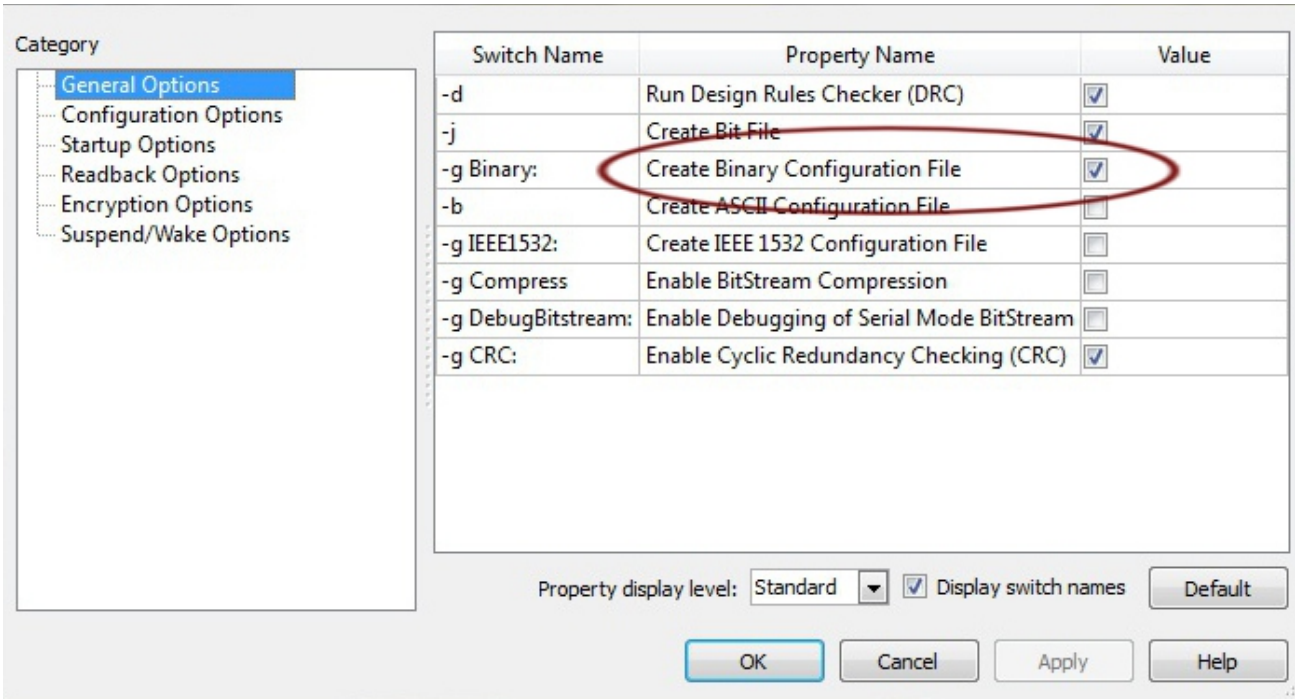
Generating Bit Stream for Neso

HDL design needs to be converted to bit stream before it can be programmed to FPGA. Neso at this time accepts only binary (.bin) bitstream created by XILINX ISE (http://www.xilinx.com/tools/webpack.htm). Once the HDL is synthesized, it is easy to create a binary bit stream out of it. Please follow the steps below to generate binary bit stream from your design using ISE Web Pack.

Step 1: Right click on the “Generate Programming File” option in “Processes” window.



Step 2: Select “Process Properties” from the pop up menu. In the dialog box, check “Create Binary Configuration File” Check box and click “Apply”.



Step 3: Click “OK” to close the dialog box. Right click on “Generate Programming File” option again and select “Run”. Now you will be able to find a “.bin” file in the project directory and that file can be used for Neso configuration.

Powering Up Neso

Neso is factory configured to be powered directly from USB port so make sure that you are using a USB port that can power the board properly. It is recommended to connect the board directly to the PC instead using a hub. It is practically very difficult to estimate the power consumption of the board, as it depends heavily on your design and the clock used. XILINX provides tools to estimate the power consumption. In any case if power from USB is not enough for your application, external supply can be applied to the board. Jumper PWRSEL should be set up properly (short pin 1-2) to use the board on external power. Neso requires three different voltages, a 3.3V, a 1.8V supplies and a 1.3V supply. On-board regulators derive these voltages from the USB/Ext power supply.

Configuring Neso Artix-7 Module

The Neso Artix-7 module can be configured by two methods,

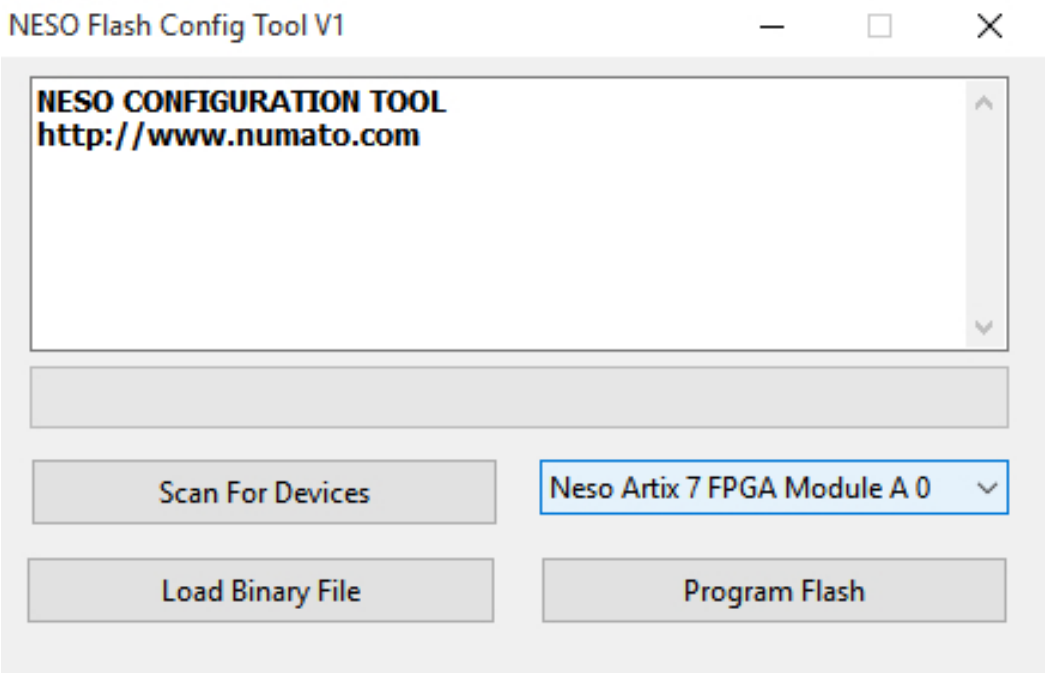
a) Using Artix-7 configuration tool through USB.

b) Using the Xilinx programming cable.

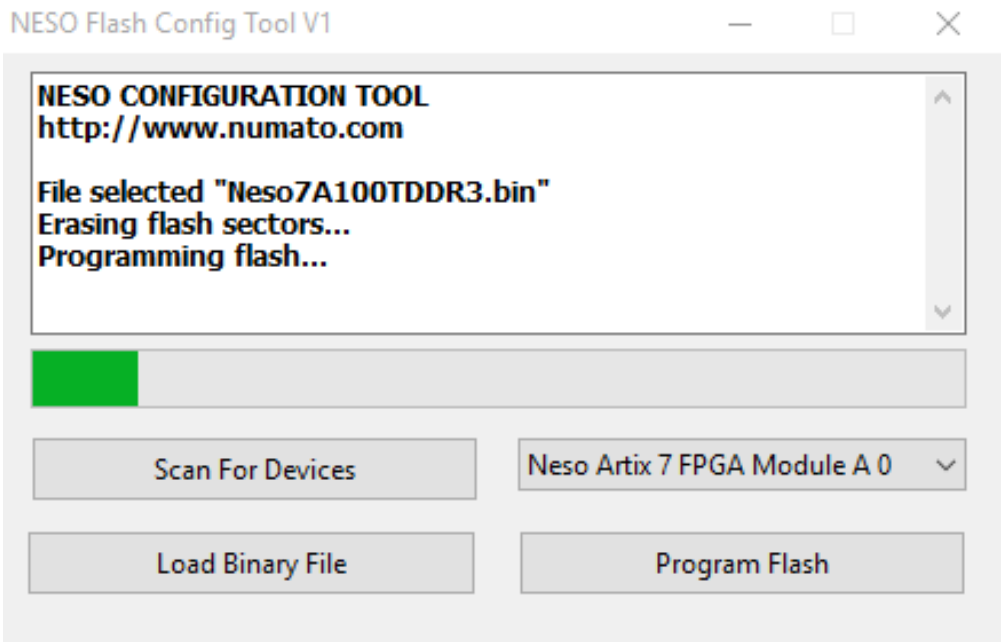
Configuring Neso using configuration tool

Neso has an on-board FTDI FT2232 device which facilitates easy reprogramming of on-board SPI flash through USB interface. The FTDI receives bit stream from the host application and program it in to the SPI Flash and lets the FPGA boot from the flash. The Neso configuration application can be downloaded from **www.numato.com** for free.

Step 1: Open Neso Config Tool. Click “Scan for Devices” if “Neso Artix-7 FPGA Module” is not detected automatically.



Step 2: Click on “Load Binary” Select the “.bin” file, then click on “Program Flash” button. Wait till “Programming Completed” appears on the screen.

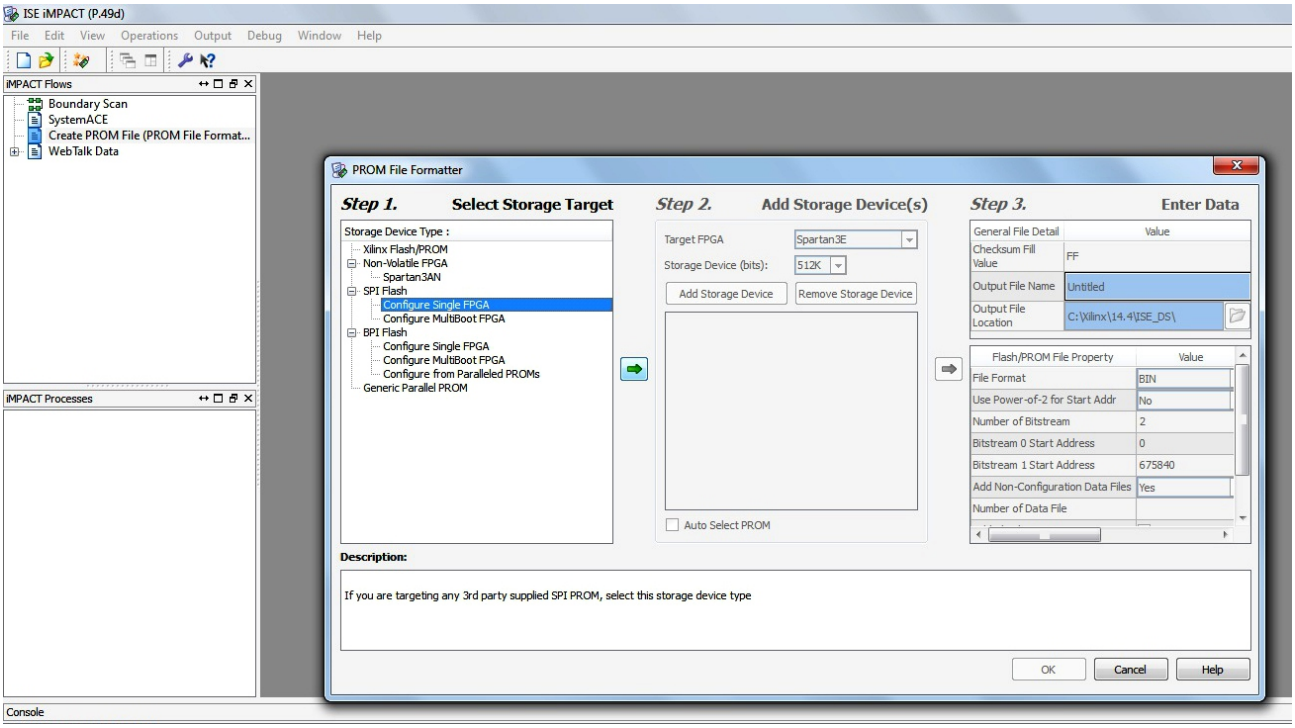


Configuring Neso using JTAG

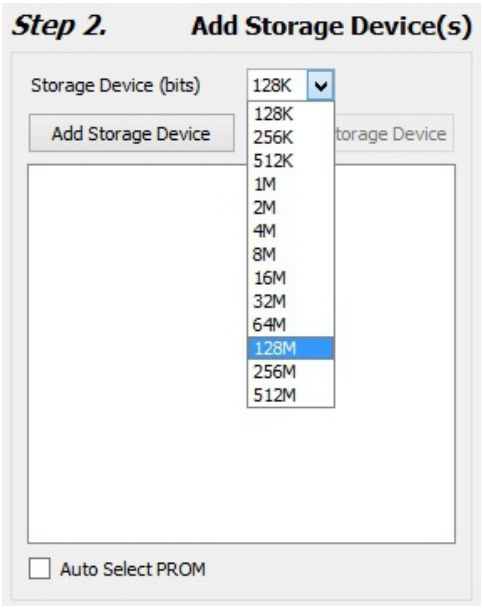
Neso Artix-7 module features an on-board JTAG connector which facilitates easy reprogramming of SRAM and on-board SPI flash through JTAG programmer like “XILINX Platform-cable usb”. Programming Neso using JTAG requires “XILINX ISE iMPACT” software which is bundled with XILINX ISE Design Suite. To program the SPI flash we need a ".mcs" file needs to be generated from the ".bit" file. Steps for generating ".mcs" file are as below. Programming FPGA SRAM does not require a “.mcs” file to be generated.

Generating ".mcs" file for Neso using ISE iMPACT

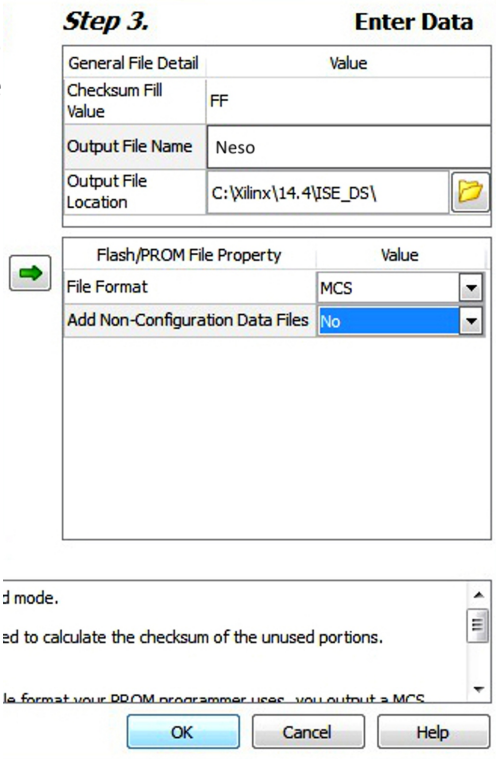
Step 1: Open ISE iMPACT. Click on “Create PROM file(PROM file formatter)”. In the dialog box, select “Configure Single FPGA” in storage device type. Then click on the green arrow on the right side.



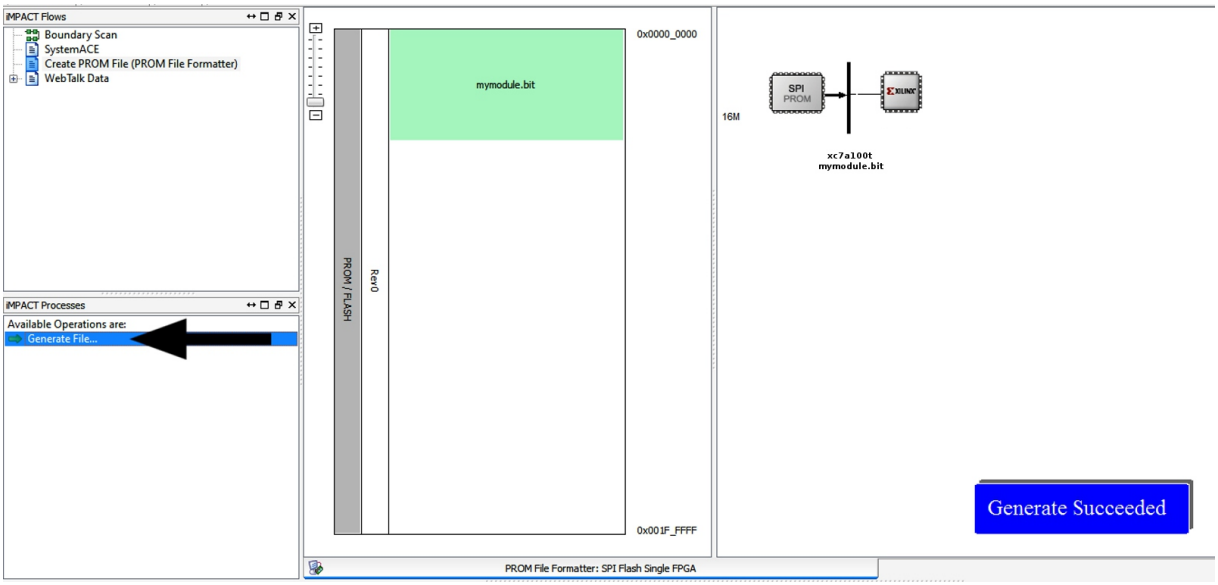
Step 2: Select 128M in Storage Device (bits).Now click on “Add Storage Device”, then the green arrow on the right side.



Step 3: Set an output file name and the output file location (the ".mcs" file will be generated at this location which will be required later for programming the FPGA), then click OK twice, then select the “.bit” file we already generated then click Open and click NO when it prompts to add another device file.

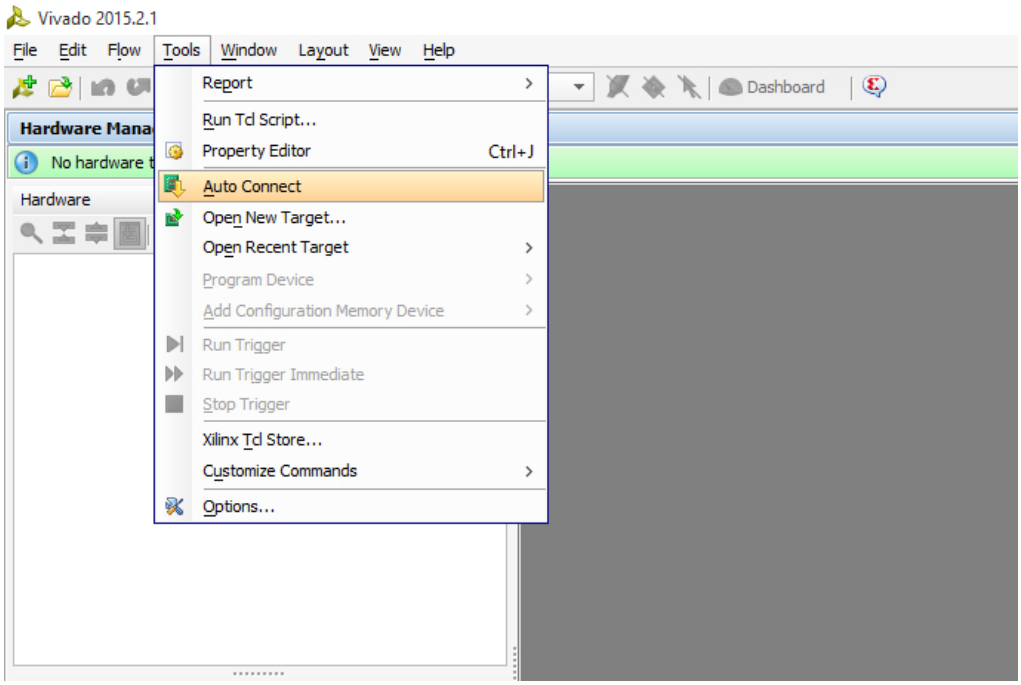


Step 4: Double click on “Generate File”. A “Generate Succeeded” will be displayed as shown in the image below if the “.mcs” the file is generated successfully.

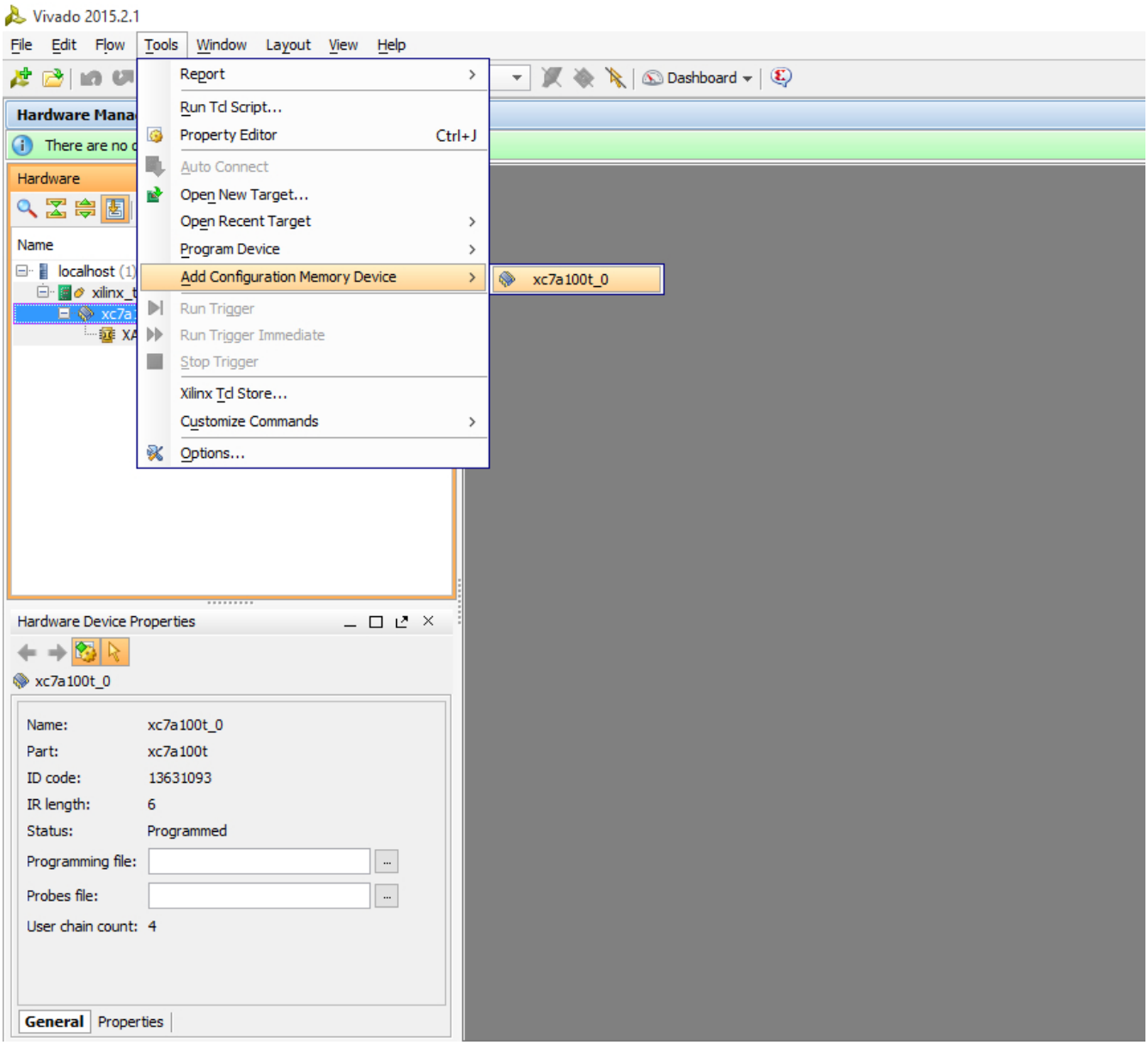


Programming FPGA using VIVADO

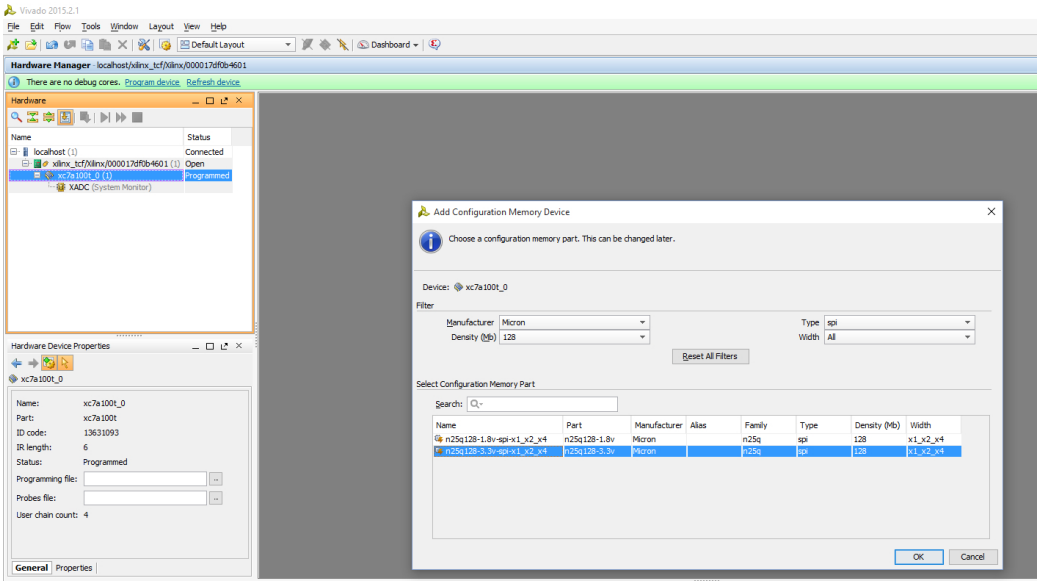
Step 1: Run VIVADO and open Hardware Manager. Select Tools -> Auto Connect.



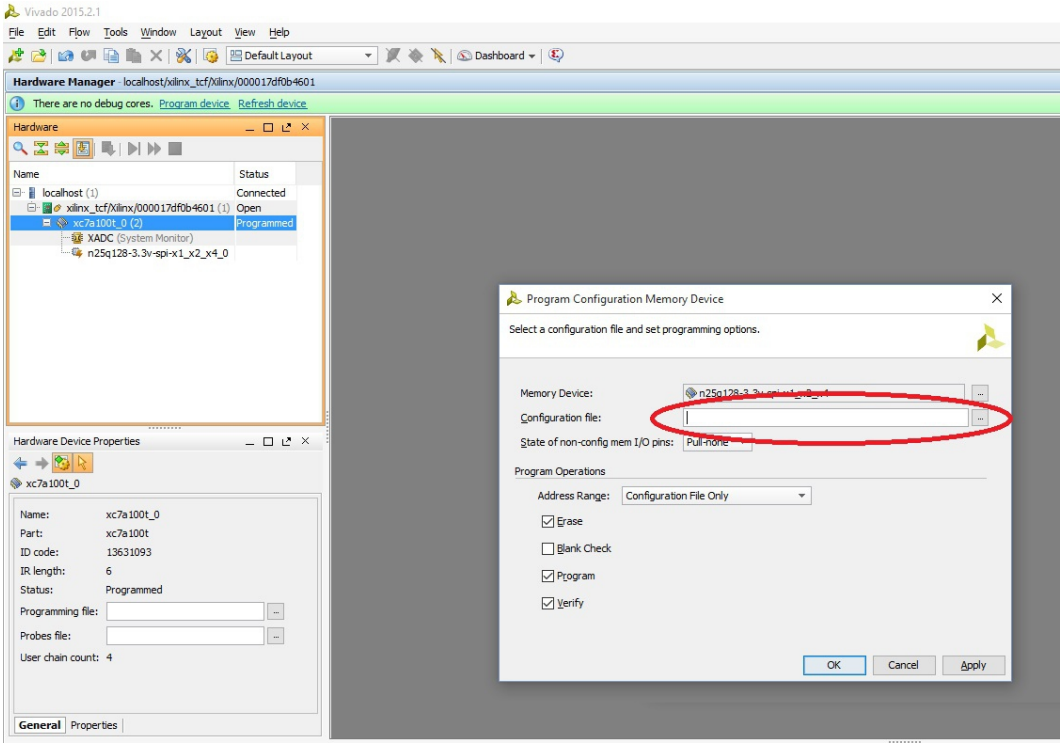
Step 2: Go to Tools, Select Add Configuration Memory Device, then the FPGA device.



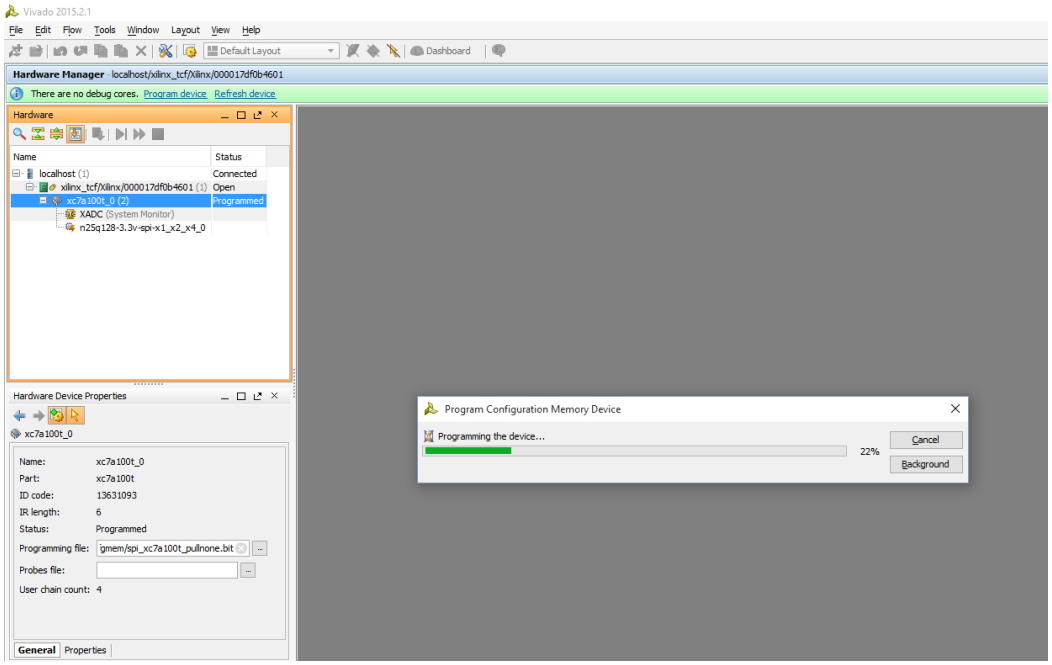
Step 3: In the dialogue box that appears, select Micron, SPI, 128Mb in the Manufacturer, Type and Density section respectively and select n25q128-3.3v. Then click OK.



Step 4: Select the configuration file (.bin) and click OK button to program.



Wait until programming completes.

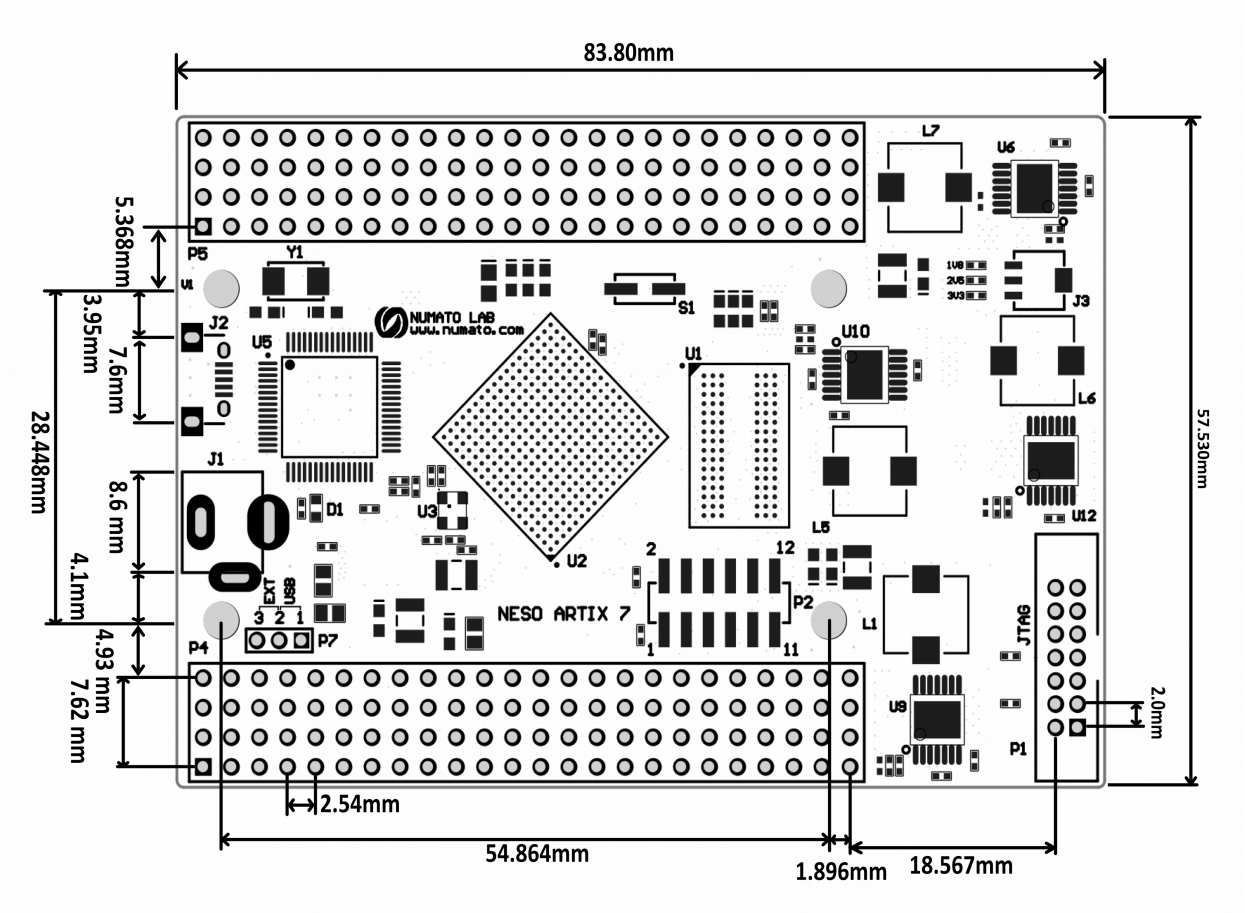


Technical Specifications

Parameter *	Value	Unit
Basic Specifications		
Number of GPIOs	148(Max)	
On-board oscillator frequency (FXO-HC536R)	100	MHz
DDR3 Capacity	2	Gb
SPI Flash Memory (N25Q128A13ESE40E)	128	Mb
Power supply voltage (USB or external)	5 – 6	V
FPGA Specifications		
Internal supply voltage relative to GND	–0.5 to 1.1	V
Auxiliary supply voltage relative to GND	–0.5 to 2.0	V
Output drivers supply voltage relative to GND	–0.5 to 3.6	V

* All parameters considered nominal. Numato Systems Pvt Ltd reserve the right to modify products without notice.

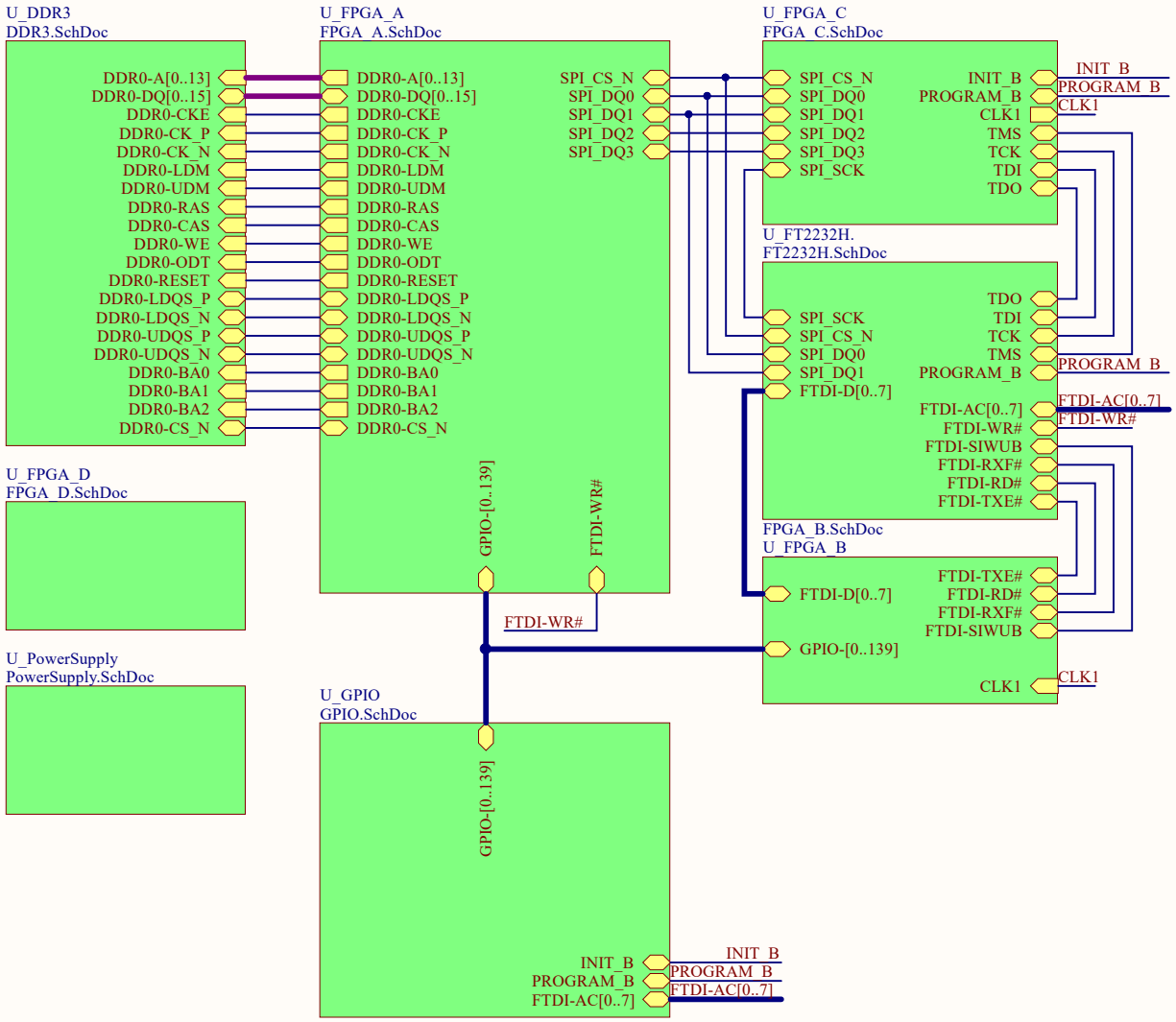
Physical Dimensions



L x W x H : 83.80mm x 57.53mm x 16mm

Schematics

See next page.



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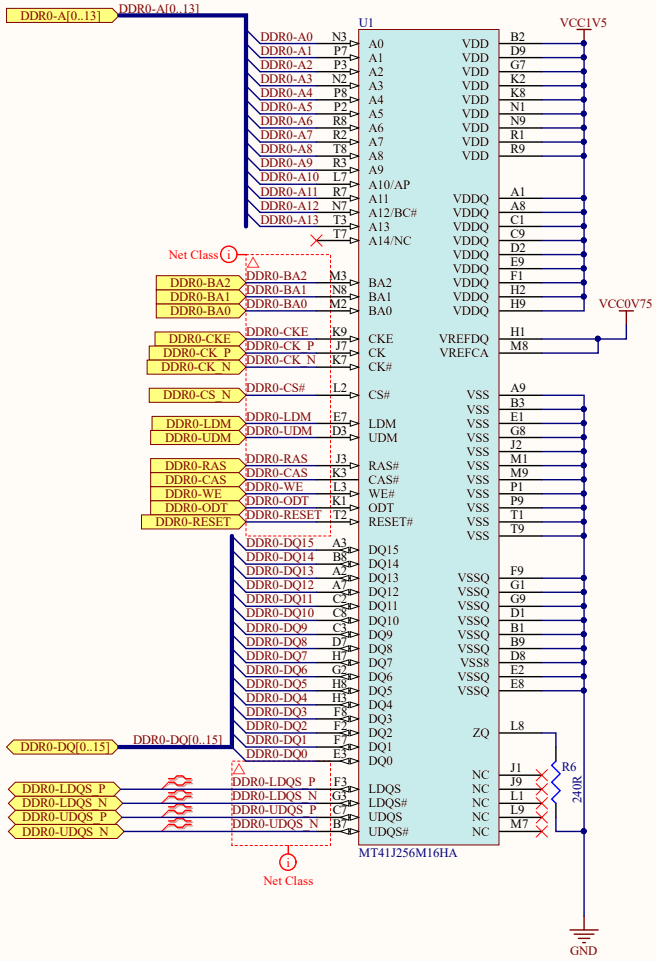
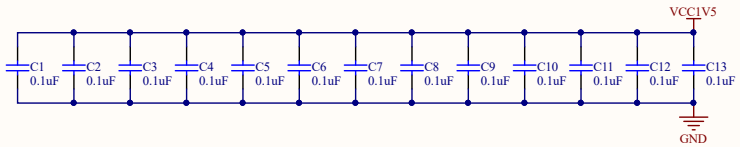
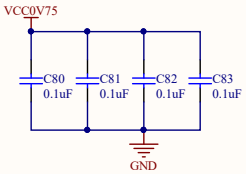
File: G:\Numato SVN\..\Mars.SchDoc		Drawn By:







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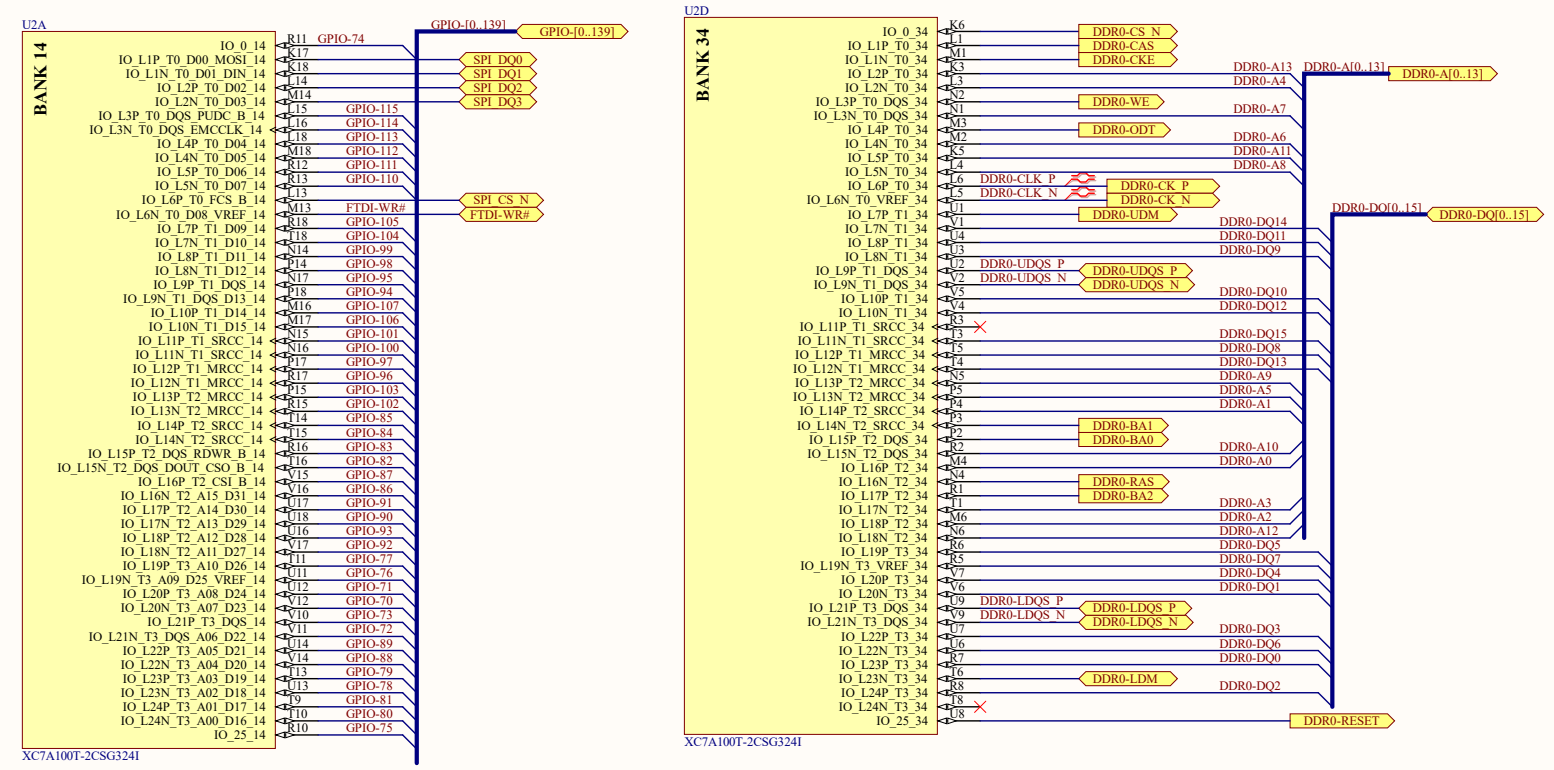

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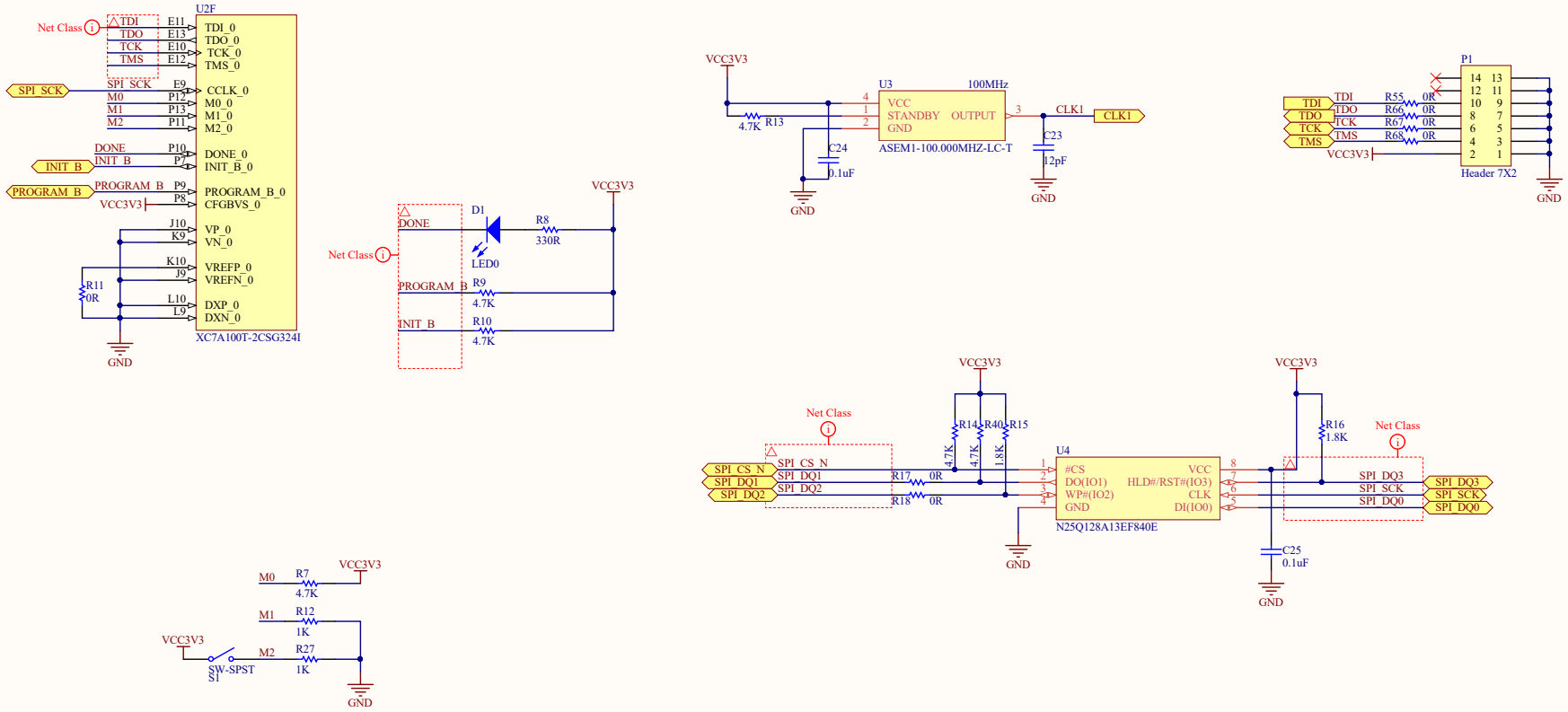

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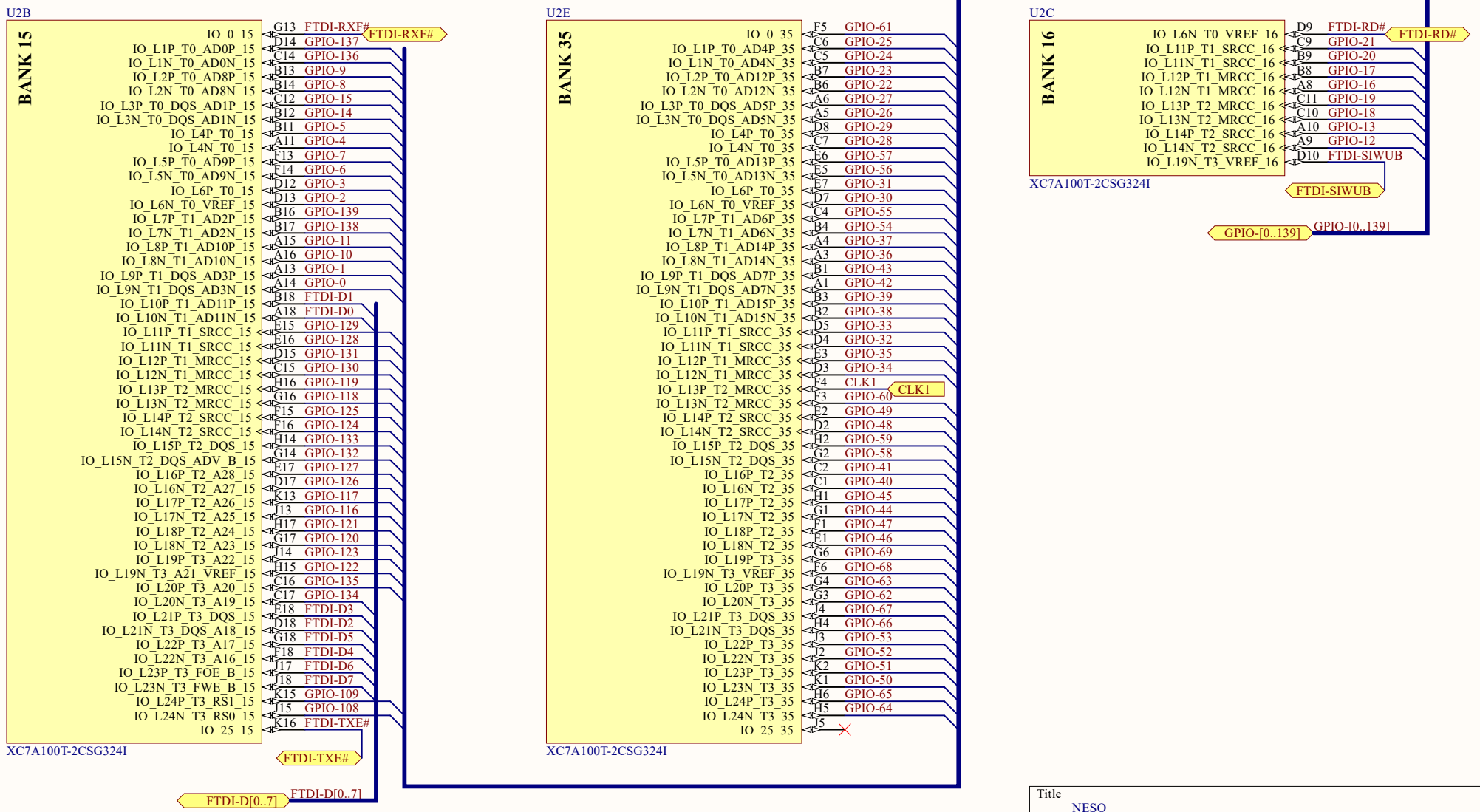

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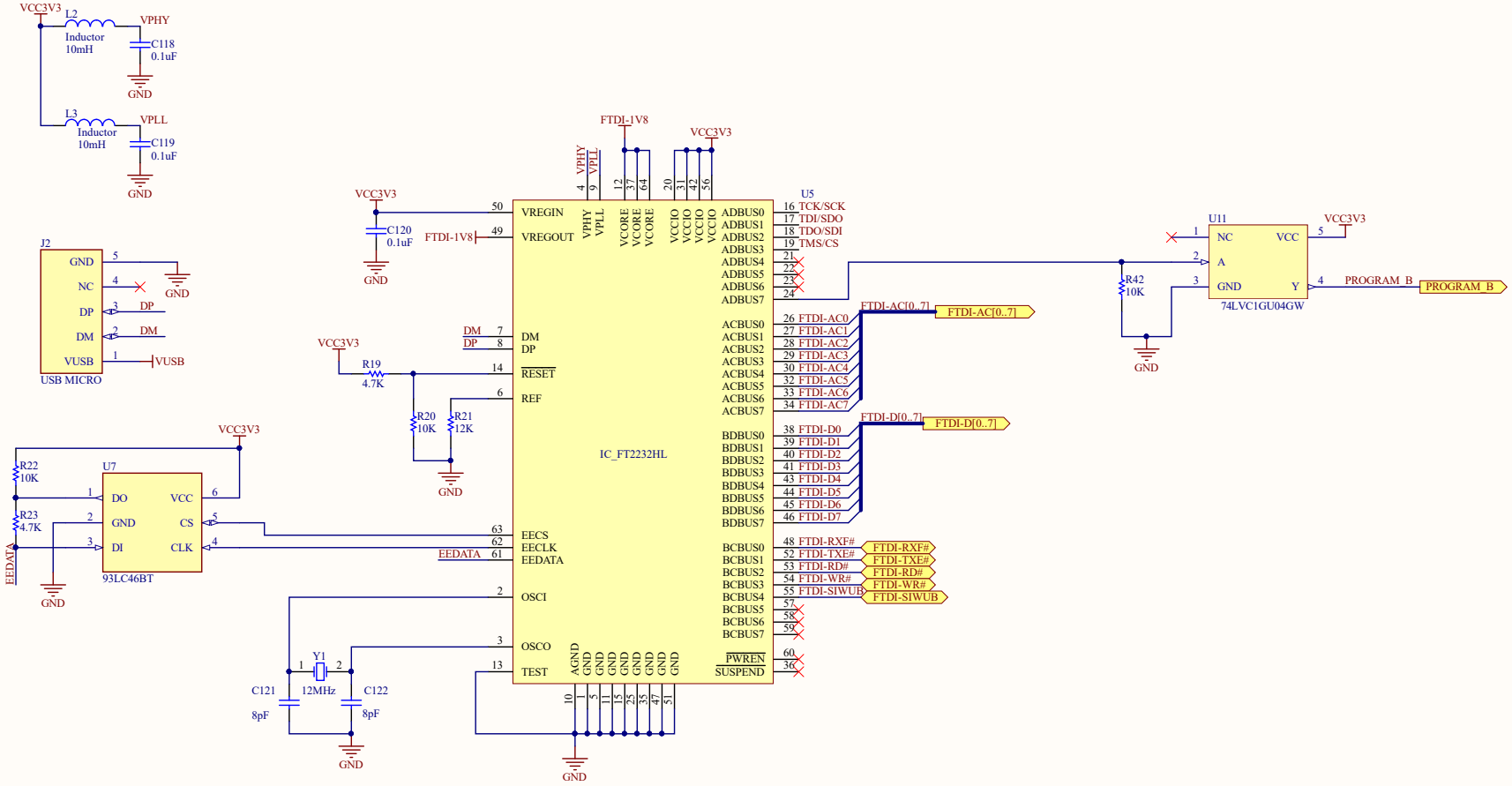

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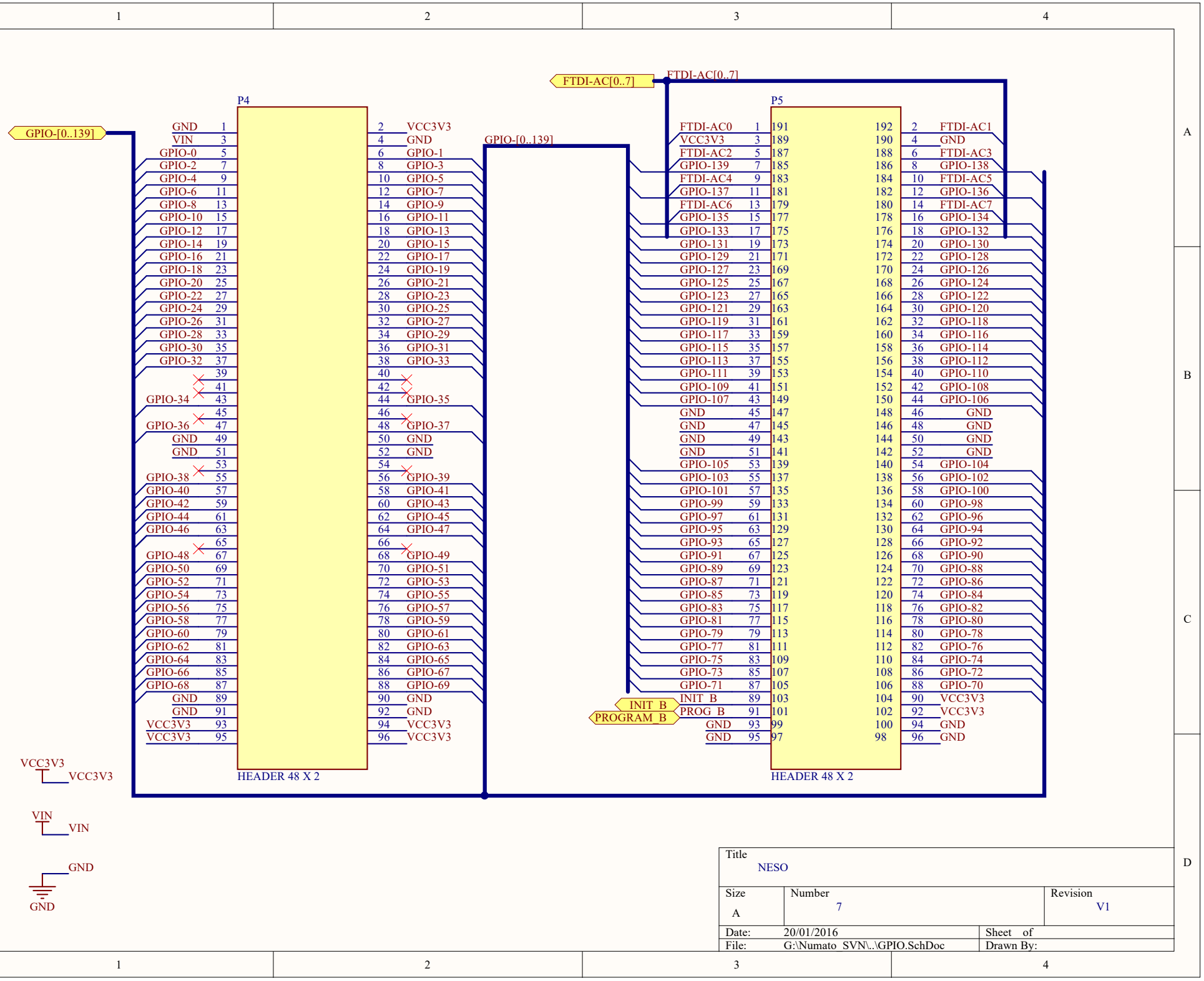
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GPIO-2 7
GPIO-4 9
GPIO-6 11
GPIO-8 13
GPIO-10 15
GPIO-12 17
GPIO-14 19
GPIO-16 21
GPIO-18 23
GPIO-20 25
GPIO-22 27
GPIO-24 29
GPIO-26 31
GPIO-28 33
GPIO-30 35
GPIO-32 37
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41
GPIO-34 43
45
GPIO-36 47
GND 49
GND 51
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GPIO-38 55
GPIO-40 57
GPIO-42 59
GPIO-44 61
GPIO-46 63
65
GPIO-48 67
GPIO-50 69
GPIO-52 71
GPIO-54 73
GPIO-56 75
GPIO-58 77
GPIO-60 79
GPIO-62 81
GPIO-64 83
GPIO-66 85
GPIO-68 87
GND 89
GND 91
VCC3V3 93
VCC3V3 95
2 VCC3V3
4 GND
6 GPIO-1
8 GPIO-3
10 GPIO-5
12 GPIO-7
14 GPIO-9
16 GPIO-11
18 GPIO-13
20 GPIO-15
22 GPIO-17
24 GPIO-19
26 GPIO-21
28 GPIO-23
30 GPIO-25
32 GPIO-27
34 GPIO-29
36 GPIO-31
38 GPIO-33
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42
44 GPIO-35
46
48 GPIO-37
50 GND
52 GND
54
56 GPIO-39
58 GPIO-41
60 GPIO-43
62 GPIO-45
64 GPIO-47
66
68 GPIO-49
70 GPIO-51
72 GPIO-53
74 GPIO-55
76 GPIO-57
78 GPIO-59
80 GPIO-61
82 GPIO-63
84 GPIO-65
86 GPIO-67
88 GPIO-69
90 GND
92 GND
94 VCC3V3
96 VCC3V3
HEADER 48 X 2
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FTDI-AC[0..7]
FTDI-AC[0..7]
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VCC3V3 3
FTDI-AC2 5
GPIO-139 7
FTDI-AC4 9
GPIO-137 11
FTDI-AC6 13
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GPIO-133 17
GPIO-131 19
GPIO-129 21
GPIO-127 23
GPIO-125 25
GPIO-123 27
GPIO-121 29
GPIO-119 31
GPIO-117 33
GPIO-115 35
GPIO-113 37
GPIO-111 39
GPIO-109 41
GPIO-107 43
GND 45
GND 47
GND 49
GND 51
GPIO-105 53
GPIO-103 55
GPIO-101 57
GPIO-99 59
GPIO-97 61
GPIO-95 63
GPIO-93 65
GPIO-91 67
GPIO-89 69
GPIO-87 71
GPIO-85 73
GPIO-83 75
GPIO-81 77
GPIO-79 79
GPIO-77 81
GPIO-75 83
GPIO-73 85
GPIO-71 87
INIT_B 89
PROG_B 91
GND 93
GND 95
191 192
189 190
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123 124
121 122
119 120
117 118
115 116
113 114
111 112
109 110
107 108
105 106
103 104
101 102
99 100
97 98
2 FTDI-AC1
4 GND
6 FTDI-AC3
8 GPIO-138
10 FTDI-AC5
12 GPIO-136
14 FTDI-AC7
16 GPIO-134
18 GPIO-132
20 GPIO-130
22 GPIO-128
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46 GND
48 GND
50 GND
52 GND
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66 GPIO-92
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72 GPIO-86
74 GPIO-84
76 GPIO-82
78 GPIO-80
80 GPIO-78
82 GPIO-76
84 GPIO-74
86 GPIO-72
88 GPIO-70
90 VCC3V3
92 VCC3V3
94 GND
96 GND
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PROGRAM_B
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Number
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Revision
V1
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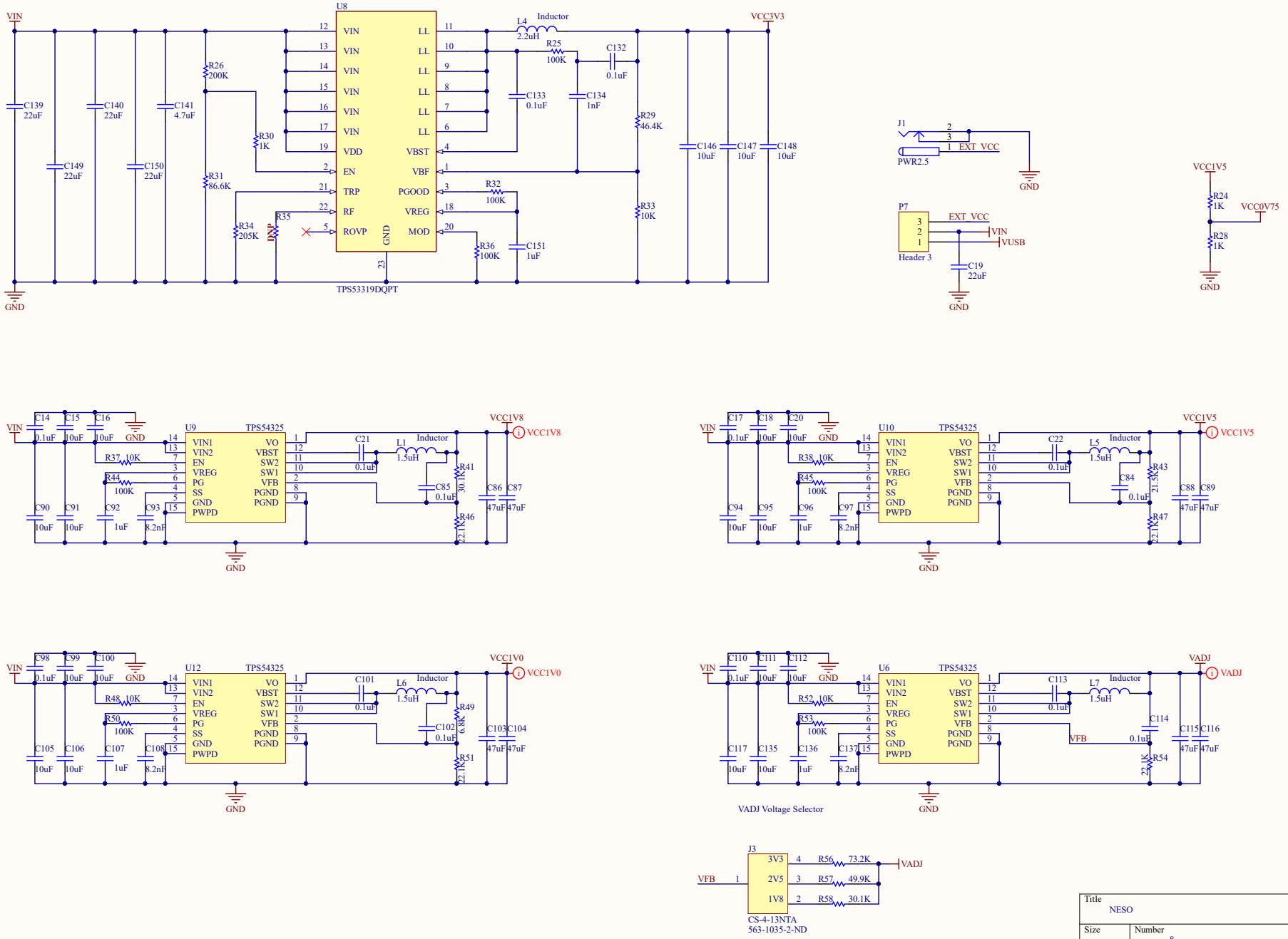

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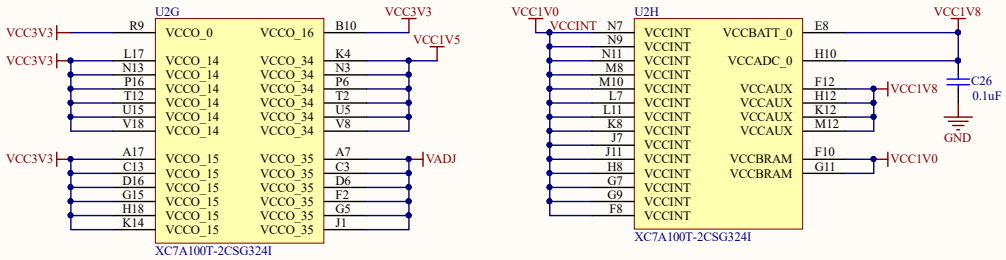

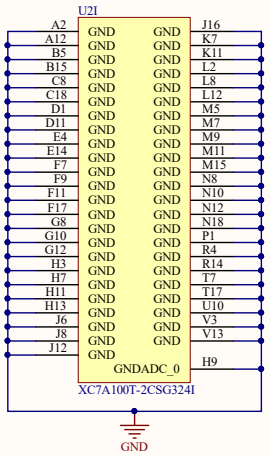

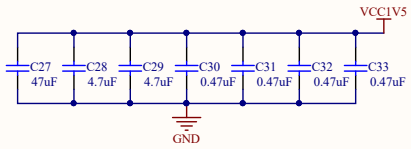

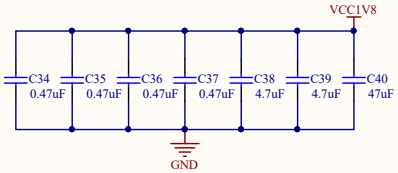

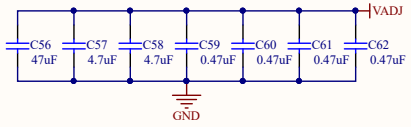

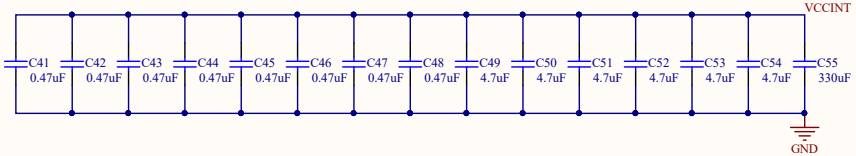

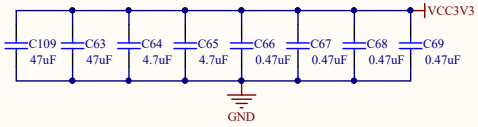

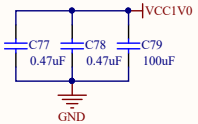

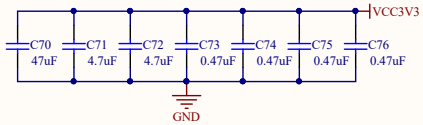

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Neso GPIO Easy Reference

HEADER P4

Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin Description
1	GND	NA	2	3V3	NA	3	VCCIN	NA	4	GND	NA
5	A14	IO_L9N_T1_DQS_AD3N_15	6	A13	IO_L9P_T1_DQS_AD3P_15	7	D13	IO_L6N_T0_VREF_15	8	D12	IO_L6P_T0_15
9	A11	IO_L4N_T0_15	10	B11	IO_L4P_T0_15	11	F14	IO_L5N_T0_AD9N_15	12	F13	IO_L5P_T0_AD9P_15
13	B14	IO_L2N_T0_AD8N_15	14	B13	IO_L2P_T0_AD8P_15	15	A16	IO_L8N_T1_AD10N_15	16	A15	IO_L8P_T1_AD10P_15
17	A9	IO_L14N_T2_SRCC_16	18	A10	IO_L14P_T2_SRCC_16	19	B12	IO_L3N_T0_DQS_AD1N_15	20	C12	IO_L3P_T0_DQS_AD1P_15
21	A8	IO_L12N_T1_MRCC_16	22	B8	IO_L12P_T1_MRCC_16	23	C10	IO_L13N_T2_MRCC_16	24	C11	IO_L13P_T2_MRCC_16
25	B9	IO_L11N_T1_SRCC_16	26	C9	IO_L11P_T1_SRCC_16	27	B6	IO_L2N_T0_AD12N_35	28	B7	IO_L2P_T0_AD12P_35
29	C5	IO_L1N_T0_AD4N_35	30	C6	IO_L1P_T0_AD4P_35	31	A5	IO_L3N_T0_DQS_AD5N_35	32	A6	IO_L3P_T0_DQS_AD5P_35
33	C7	IO_L4N_T0_35	34	D8	IO_L4P_T0_35	35	D7	IO_L6N_T0_VREF_35	36	E7	IO_L6P_T0_35
37	D4	IO_L11N_T1_SRCC_35	38	D5	IO_L11P_T1_SRCC_35	39	-	-	40	-	-
41	-	-	42	-	-	43	D3	IO_L12N_T1_MRCC_35	44	E3	IO_L12P_T1_MRCC_35
45	-	-	46	-	-	47	A3	IO_L8N_T1_AD14N_35	48	A4	IO_L8P_T1_AD14P_35
49	GND	NA	50	GND	NA	51	GND	NA	52	GND	NA
53	-	-	54	-	-	55	B2	IO_L10N_T1_AD15N_35	56	B3	IO_L10P_T1_AD15P_35
57	C1	IO_L16N_T2_35	58	C2	IO_L16P_T2_35	59	A1	IO_L9N_T1_DQS_AD7N_35	60	B1	IO_L9P_T1_DQS_AD7P_35
61	G1	IO_L17N_T2_35	62	H1	IO_L17P_T2_35	63	E1	IO_L18N_T2_35	64	F1	IO_L18P_T2_35
65	-	-	66	-	-	67	D2	IO_L14N_T2_SRCC_35	68	E2	IO_L14P_T2_SRCC_35
69	K1	IO_L23N_T3_35	70	K2	IO_L23P_T3_35	71	J2	IO_L22N_T3_35	72	J3	IO_L22P_T3_35
73	B4	IO_L7N_T1_AD6N_35	74	C4	IO_L7P_T1_AD6P_35	75	E5	IO_L5N_T0_AD13N_35	76	E6	IO_L5P_T0_AD13P_35
77	G2	IO_L15N_T2_DQS_35	78	H2	IO_L15P_T2_DQS_35	79	F3	IO_L13N_T2_MRCC_35	80	F5	IO_0_35
81	G3	IO_L20N_T3_35	82	G4	IO_L20P_T3_35	83	H5	IO_L24N_T3_35	84	H6	IO_L24P_T3_35
85	H4	IO_L21N_T3_DQS_35	86	J4	IO_L21P_T3_DQS_35	87	F6	IO_L19N_T3_VREF_35	88	G6	IO_L19P_T3_35
89	GND	NA	90	GND	NA	91	GND	NA	92	GND	NA
93	3V3	NA	94	3V3	NA	95	3V3	NA	96	3V3	NA

BANK 35 IO

HEADER P5

Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Artix-7 (CSG324) Pin No.	Pin Description
1	FTDI-26	ACBUS0	2	FTDI-27	ACBUS1	3	3V3	NA	4	GND	NA
5	FTDI-28	ACBUS2	6	FTDI-29	ACBUS3	7	B16	IO_L7P_T1_AD2P_15	8	B17	IO_L7N_T1_AD2N_15
9	FTDI-30	ACBUS4	10	FTDI-32	ACBUS5	11	D14	IO_L1P_T0_AD0P_15	12	C14	IO_L1N_T0_AD0N_15
13	FTDI-33	ACBUS6	14	FTDI-34	ACBUS7	15	C16	IO_L20P_T3_A20_15	16	C17	IO_L20N_T3_A19_15
17	H14	IO_L15P_T2_DQS_15	18	G14	IO_L15N_T2_DQS_ADV_B_15	19	D15	IO_L12P_T1_MRCC_15	20	C15	IO_L12N_T1_MRCC_15
21	E15	IO_L11P_T1_SRCC_15	22	E16	IO_L11N_T1_SRCC_15	23	E17	IO_L16P_T2_A28_15	24	D17	IO_L16N_T2_A27_15
25	F15	IO_L14P_T2_SRCC_15	26	F16	IO_L14N_T2_SRCC_15	27	J14	IO_L19P_T3_A22_15	28	H15	IO_L19N_T3_A21_VREF_15
29	H17	IO_L18P_T2_A24_15	30	G17	IO_L18N_T2_A23_15	31	H16	IO_L13P_T2_MRCC_15	32	G16	IO_L13N_T2_MRCC_15
33	K13	IO_L17P_T2_A26_15	34	J13	IO_L17N_T2_A25_15	35	L15	IO_L3P_T0_DQS_PUDC_B_14	36	L16	IO_L3N_T0_DQS_EMCCLK_14
37	L18	IO_L4P_T0_D04_14	38	M18	IO_L4N_T0_D05_14	39	R12	IO_L5P_T0_D06_14	40	R13	IO_L5N_T0_D07_14
41	K15	IO_L24P_T3_RS1_15	42	J15	IO_L24N_T3_RS0_15	43	M16	IO_L10P_T1_D14_14	44	M17	IO_L10N_T1_D15_14
45	GND	NA	46	GND	NA	47	GND	NA	48	GND	NA
49	GND	NA	50	GND	NA	51	GND	NA	52	GND	NA
53	R18	IO_L7P_T1_D09_14	54	T18	IO_L7N_T1_D10_14	55	P15	IO_L13P_T2_MRCC_14	56	R15	IO_L13N_T2_MRCC_14

57	N15	IO_L11P_T1_SRCC_14	58	N16	IO_L11N_T1_SRCC_14	59	N14	IO_L8P_T1_D11_14	60	P14	IO_L8N_T1_D12_14
61	P17	IO_L12P_T1_MRCC_14	62	R17	IO_L12N_T1_MRCC_14	63	N17	IO_L9P_T1_DQS_14	64	P18	IO_L9N_T1_DQS_D13_14
65	U16	IO_L18P_T2_A12_D28_14	66	V17	IO_L18N_T2_A11_D27_14	67	U17	IO_L17P_T2_A14_D30_14	68	U18	IO_L17N_T2_A13_D29_14
69	U14	IO_L22P_T3_A05_D21_14	70	V14	IO_L22N_T3_A04_D20_14	71	V15	IO_L16P_T2_CSI_B_14	72	V16	IO_L16N_T2_A15_D31_14
73	T14	IO_L14P_T2_SRCC_14	74	T15	IO_L14N_T2_SRCC_14	75	R16	IO_L15P_T2_DQS_RDWR_B_14	76	T16	IO_L15N_T2_DQS_DOUT_CSO_B_14
77	T9	IO_L24P_T3_A01_D17_14	78	T10	IO_L24N_T3_A00_D16_14	79	T13	IO_L23P_T3_A03_D19_14	80	U13	IO_L23N_T3_A02_D18_14
81	T11	IO_L19P_T3_A10_D26_14	82	U11	IO_L19N_T3_A09_D25_VREF_14	83	R10	IO_25_14	84	R11	IO_0_14
85	V10	IO_L21P_T3_DQS_14	86	V11	IO_L21N_T3_DQS_A06_D22_14	87	U12	IO_L20N_T3_A07_D23_14	88	V12	IO_L20P_T3_A08_D24_14
89	INIT_B	INIT_B_0	90	3V3	NA	91	PROG_B	PROGRAM_B_0	92	3V3	NA
93	GND	NA	94	GND	NA	95	GND	NA	96	GND	NA